

WHAT IS CLAIMED IS:

1. For use in a wide-issue pipelined processor, a mechanism
2 for reducing pipeline stalls between conditional branches,
3 comprising:

4 a mispredict program counter (PC) generator that generates a
5 mispredict PC value for each conditional branch instruction in a
6 pipeline of said processor; and

7 mispredict PC storage, coupled to said mispredict PC
8 generator, that stores said mispredict PC value at least until a
9 resolution of said conditional branch instruction occurs and makes
10 said mispredict PC value available to a PC of said processor if
11 said resolution results in a mispredict condition.

2. The mechanism as recited in Claim 1 wherein said
mispredict PC generator is associated with a static branch
predictor of said processor.

3. The mechanism as recited in Claim 1 wherein said
2 mispredict PC generator generates a branch prediction and said
3 mispredict PC value in a single clock cycle.

4. The mechanism as recited in Claim 3 wherein said branch
2 prediction is employed to prefetch instructions.

5. The mechanism as recited in Claim 1 wherein a mispredict
2 PC queue of said mispredict PC storage has at least as many slots
3 as said pipeline has stages.

6. The mechanism as recited in Claim 1 wherein said
2 mispredict PC value moves through registers of said mispredict PC
3 storage as said conditional branch instruction moves through stages
4 in said pipeline.

7. The mechanism as recited in Claim 1 wherein said
resolution occurs in an execution stage of said pipeline.

8. The mechanism as recited in Claim 1 wherein said
processor is a digital signal processor.

9. For use in a wide-issue pipelined processor, a method of
2 reducing pipeline stalls between conditional branches, comprising:
3 generating a mispredict program counter (PC) value for each
4 conditional branch instruction in a pipeline of said processor; and
5 storing said mispredict PC value at least until a resolution
6 of said conditional branch instruction occurs; and
7 making said mispredict PC value available to a PC of said
8 processor if said resolution results in a mispredict condition.

10. The method as recited in Claim 9 wherein said mispredict
PC generator is associated with a static branch predictor of said
processor.

11. The method as recited in Claim 9 wherein said generating
is carried out in a single clock cycle, said method further
comprising generating a branch prediction in a single clock cycle.

12. The method as recited in Claim 11 further comprising
2 employing said branch prediction to prefetch instructions.

13. The method as recited in Claim 9 wherein a mispredict PC
2 queue of said mispredict PC storage has at least as many slots as
3 said pipeline has stages.

14. The method as recited in Claim 9 further comprising
2 moving said mispredict PC value through registers in said
3 mispredict PC storage as said conditional branch instruction moves
4 through stages in said pipeline.

15. The method as recited in Claim 9 wherein said resolution
2 occurs in an execution stage of said pipeline.

16. The method as recited in Claim 9 wherein said processor
2 is a digital signal processor.

17. A digital signal processor, comprising:

2 a pipeline having stages capable of executing conditional
3 branch instructions;

4 a wide-issue instruction issue unit;

5 a mispredict program counter (PC) generator that generates a
6 mispredict PC value for each conditional branch instruction in said
7 pipeline; and

8 mispredict PC storage, coupled to said mispredict PC
9 generator, that stores said mispredict PC value at least until a
10 resolution of said conditional branch instruction occurs and makes
11 said mispredict PC value available to a PC of said DSP if said
12 resolution results in a mispredict condition.

18. The DSP as recited in Claim 17 wherein said mispredict PC
generator is associated with a static branch predictor in said
instruction issue unit.

19. The DSP as recited in Claim 17 wherein said mispredict PC
2 generator generates a branch prediction and said mispredict PC
3 value in a single clock cycle.

20. The DSP as recited in Claim 19 wherein said branch
2 prediction is employed to prefetch instructions.

21. The DSP as recited in Claim 17 wherein a mispredict PC
2 queue of said mispredict PC storage has at least as many slots as
3 said pipeline has said stages.

22. The DSP as recited in Claim 17 wherein said mispredict PC
2 value moves through registers in said mispredict PC storage as said
3 conditional branch instruction moves through said stages.

23. The DSP as recited in Claim 17 wherein said resolution
2 occurs in an execution stage of said pipeline.